

HA11423

T-77-07-11

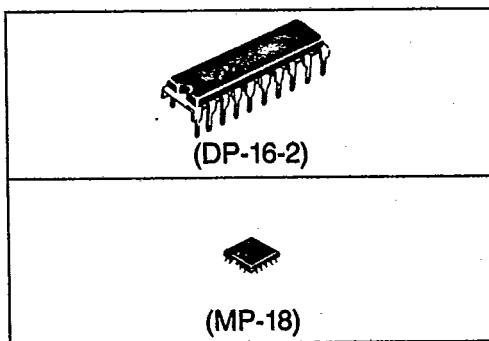
Color TV Deflection Signal Processor

Functions

- Sync separator
- Horizontal AFC
- Horizontal oscillator
- X-ray radiation protector
- Vertical oscillator
- Vertical blanking pulse generator

Features

- On-chip blanking circuit: Simplifies output circuit design
- Constant discharge current: No vertical output linearity adjustment
- Horizontal oscillator frequency limiter: No X-ray protector malfunction
- Hold-type operation for X-ray protector
- Less reduction of impedance from frost between pins



Ordering Information

Type No.	Package
HA11423	300 mil 18 pin plastic DIP (DP-16-2)
HA11423MP	18 pin plastic QFI (MP-18)

Table 1 External Components

Part No.	Recommended Value	Larger Than Recommended Value	Smaller Than Recommended Value
R ₁₁₄ (pin 1)	100 Ω	A small h _{FE} at the output transistor may delay the leading edge of the blanking pulse	—
C ₈ (pin 2)	33,000 pF	May cause ringing during the first half of the vertical output scan	Horizontal component leakage increases; may cause abnormal oscillation; may delay leading edge of blanking pulse
C ₁₄ (output capacitor)	180 pF	May cause blocking oscillation	May cause high-frequency oscillation
R ₁₀₁ , C ₃₃ (filter at pin 5)	120 Ω, 330 μF		May cause interlacing
Output transistor emitter resistor	0 Ω	A small h _{FE} at the output transistor may delay the leading edge of the blanking pulse	—
R ₁₀₉ (oscillation time constant)	24 kΩ	A small h _{FE} at the output transistor may delay the leading edge of the blanking pulse	—



Operating Principles

The HA11423 consists of a sync separation circuit, a horizontal AFC circuit, a voltage controlled oscillator (VCO), a pulse shaping circuit, a high-voltage protection circuit, a vertical oscillator, a driver, and a vertical blanking circuit.

Sync Separation Circuit

The peak-detection-type sync separator is connected to the PIF section's power supply by C₂ and R₁₀₂ (figure 1) for excellent supply voltage ripple rejection.

R₁₀₂ and R₁₀₃ determine the sync separation slice level and the dynamic range.

The sync separation output is internally connected to the phase detection circuit and is output as a positive pulse at pin 8.

The sync tip DC level can be adjusted between 2.1 V and 8.5 V by changing R₁₀₂ and R₁₀₃.

Horizontal AFC Circuit/Free-Running Frequency Limiter

The horizontal AFC circuit consists of a fully balanced pulse-width-type phase detector and an external lowpass filter (figure 2).

The free-running frequency limiter includes Q₂₅ limit circuit to keep the horizontal osc frequency down to 14.9 kHz typ. The limiter is usually cut off because Q₂₅ is reverse biased. It operates when the voltage at pin 12 goes down. During the vertical operation, the blanking signal releases the limiter to prevent the pull-in range from decreasing.

The lowpass filter in the AFC circuit consists of R₁₂₆, R₁₂₇, C₁₅, and C₁₇. The loop gain is internally adjusted to f_c = 750 Hz/μs typ.

The AC loop gain is determined by R₁₂₆ and R₁₂₇. It can be optimized by adjusting the characteristics of the screen's upper side curl, skew, and noise under weak field.

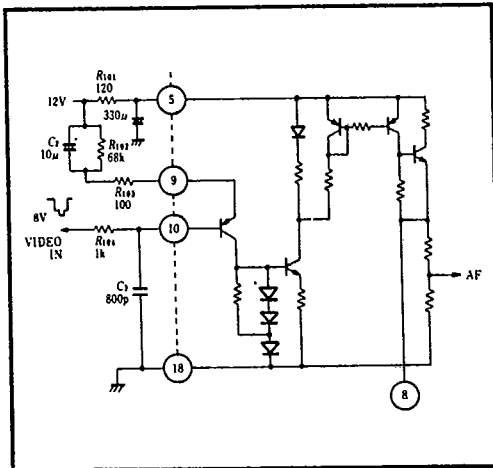


Figure 1 Sync Separation Circuit

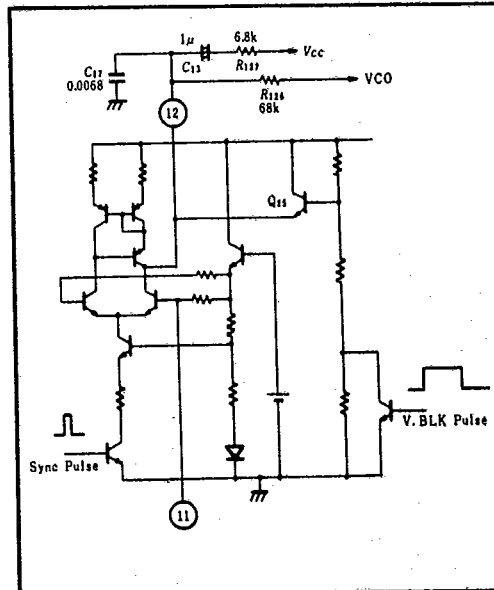


Figure 2 Horizontal AFC Circuit and Free-Running Frequency Limiter



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The recommended values are:

- $R_{126} = 68 \text{ k}\Omega$
- $R_{127} = 4.7\text{--}6.8 \text{ k}\Omega$
- $C_{17} = 6800 \text{ pF}$
- $C_{13} = 1 \mu\text{F}$

Voltage Controlled Oscillator

The VCO is a differential CR oscillator. The external resistor and capacitor at pin 13 determine the charging time constant (figure 3). The external capacitor at pin 13 and internal resistor R_{23} determine the discharging time. R_{27} , R_{28} , and R_{29} determine the threshold voltage.

Pulse Shaping Circuit/High-Voltage Protection Circuit

The pulse shaping circuit shapes the saw-tooth pulse waveform to a rectangular pulse ($25 \mu\text{s}$ typ), which is input to the output drive transistor (figure 4).

The high-voltage protection circuit detects

excessive voltage through pin 16. It stops the horizontal output pulse by turning Q_{54} on to inhibit the output transistor. Q_{53} holds the transistor in the non-operating state.

Vertical Oscillator

The vertical oscillator uses the differential amplifier made up of Q_{61} and Q_{62} (figure 5).

The Q_{66} emitter voltage determines the top voltage level ($2/3 V_{CC}$).

The ratio of R_{106} to ($R_{107} + R_{108}$), the external resistors at pin 6 determine the bottom voltage level. If the bottom voltage is ($1/3 V_{CC} - V_{BE}(Q_{60})$) or less, oscillation stops. For C_7 , the capacitor at pin 3, use $1 \mu\text{F}$ or less.

Vertical Driver/Blanking Circuit

The vertical driver supplies drive current to pin 1 (figure 6). DC and AC feedback at pin 2 provides equivalence of the differential amplifier.

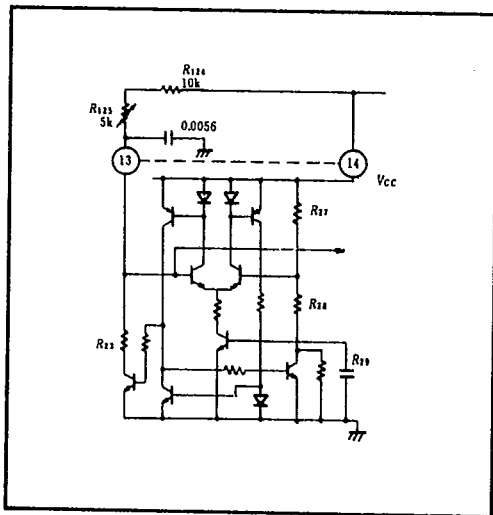


Figure 3 Horizontal Oscillation Circuit

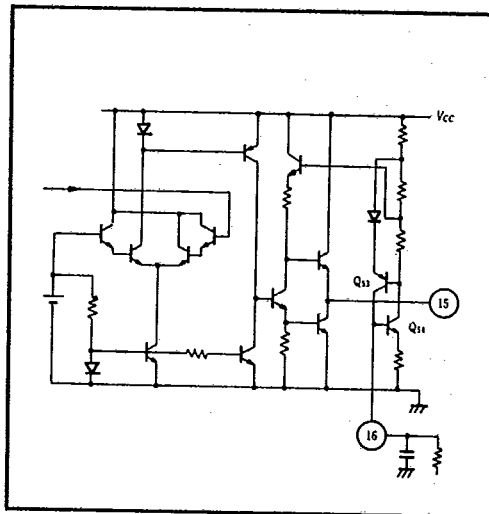


Figure 4 Pulse Shaping Circuit and High-Voltage Protection Circuit



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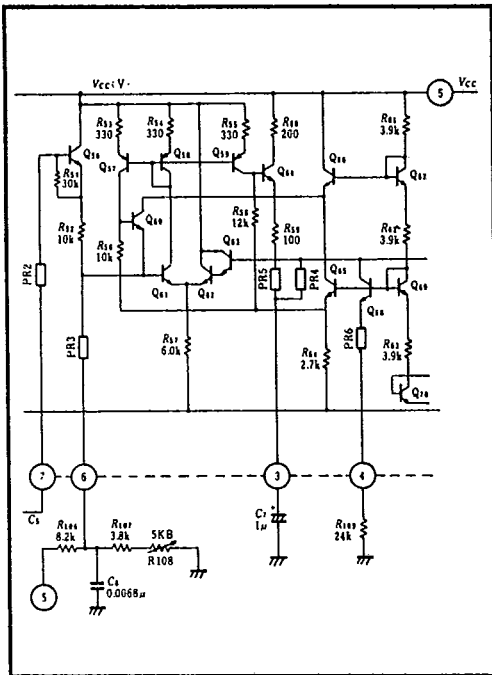


Figure 5 Vertical Oscillator

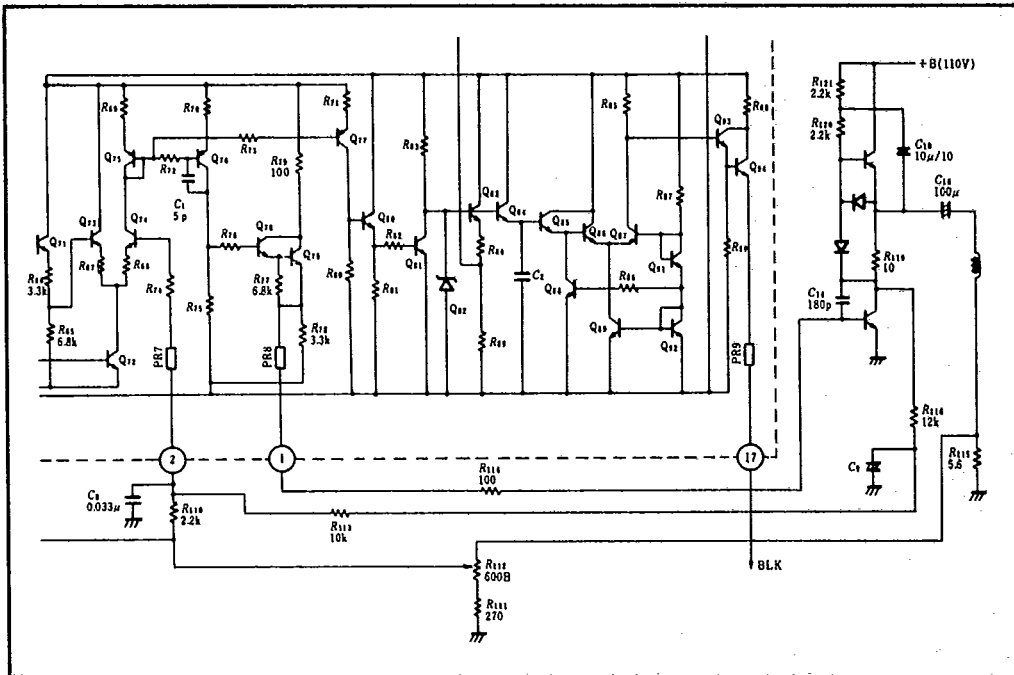


Figure 6 Vertical Driver and Blanking Circuit



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Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Vertical Supply Voltage	V_{CC} (V)	16	V
Horizontal Supply Current	I_{CC} (H)	25	mA
Vertical Output Current	I_{OV}	15	mA
Horizontal Output Current	I_{OH}	15	mA
Power Dissipation ($T_a = 75^\circ\text{C}$)	P_T	500	mW
Operating Temperature	T_{opr}	-20 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit
Horizontal DC Loop Gain	f_c	—	750	—	Hz/ μs
Horizontal Osc Frequency	f_{OH}	14.734	15.734	16.734	kHz
Horizontal Pull-In Range	f_{PH}	450	650	—	Hz
Horizontal Output Pulse Width	t_{NW}	22.5	25.0	27.5	μs
Trigger Gate Voltage	V_{GT}	0.65	0.72	0.79	V
Vertical Osc Frequency	f_{OV}	50	55	60	Hz
Vertical Blanking Pulse Delay Time (Note 1)	t_{BLK}	-10	40	180	μs
Quiescent Sync Input Horizontal Frequency (Note 2)	$f_{OH(L)}$	14.5	14.9	—	kHz

Notes: 1. Delay from vertical output blanking threshold

2. Minimum frequency under quiescent sync signal input

